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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,475	03/26/2004	Tetsu Hasegawa	251144US2	8330

22850 7590 06/25/2007

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EXAMINER	
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ART UNIT	PAPER NUMBER
2117	

NOTIFICATION DATE	DELIVERY MODE
06/25/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/809,475	HASEGAWA ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *5,10 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are present within this instant examination, in response to applicant's response on 3/13/2007 to the examination mailed to applicant on 9/13/2006. Claims 19 and 20 have been withdrawn and as such may not be given further consideration within this instant examination; applicant elected claims 1-18 without traverse.

Priority

Priority is acknowledged it 03/26/2003 as used within the prior examination.

Double Patenting

Acknowledgment is made that the applicant with respect to U.S. Patent Application 10426657 and this application, U.S. Patent Application 10809475, has filed a terminal disclaimer.

Response to Arguments

Applicant's arguments filed 3/13/2007 have been fully considered but they are not persuasive. Applicant argues that Coteet (U.S. Patent 6671839 B1) does not test the test result compression unit as defined in amended claim 1. The examiner would like to direct the applicant specifically to column 1 lines 20-26, as relied upon within the prior examination, wherein it states "the output can be analyzed by compressing the test response into a signature register and then comparing the signature obtained with an expected signature." It is believed that Coteet does teach the compression unit as claimed within the application since a compressor must be present and connected to the output stages of the scan chains used within scan testing (column 1 lines 14 of

Coteet) to perform the compressing of the test responses into signatures that are compared to expected signatures of the test patterns as indicated within column 1 of Coteet. The examiner maintains the prior rejection since all limitations as understood are taught by Coteet with respect to claim 1 as it is written.

Claim Objections

Claims 5, 10, and 14 objected to because of the following informalities: within the parallel to serial limitation, "unit" within "the data compression unit" should be changed to "units" to indicate the relation with the "compression units" within the prior limitation. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, it is unclear to the examiner what the test patterns within the test pattern generation unit within the second limitation of the claim are transformed into, wherein the claim states "a test pattern generation unit configured to transform the test patterns as scanning test pattern for feeding into the scan chains." Further it is unclear if the test scanning test patterns feed into the scan chains within the second limitation are different or are the same as the test patters the scan chains is claimed to be configured to shift in from the first limitation of the claim.

Additionally, It is the examiner's understanding from the specification that applicant intended to indicate within the third limitation of the claim: "... **and** to compare the resulting compressed test result signatures **of each of** the scan chains in order to allow one-to-one mapping to **identify** the scan chain which fails to **have a** matching compressed test result signature corresponding to each scan chain **expected signature**." This is the understanding since as the claim stands the compressed test result signatures are being compared to the physical circuitry of the scan chains themselves, which is unclear to the examiner. Examiner notes claims 2 and 3 respectfully claim the comparing an output to an expected and failure scan chain identification determination from the comparing. Examiner would like to point out while the M.P.E.P. (see M.P.E.P. 2111 [R-5] Claim Interpretation; Broadest Reasonable Interpretation) requires that the examiner give "the broadest reasonable interpretation" the claims "consistent with the specification" it also warns that "reading a claim in light of the specification, to thereby interpret limitations explicitly recited in the claim, is a quite different thing from reading limitations of the specification into a claim, to thereby narrow the scope of the claim by implicitly adding disclosed limitations which have no express basis in the claim." The claims must stand on their own.

As per claim 5, it is unclear to the examiner if the selected test results selected in order (sequentially) by the selector are provided in parallel to all the compression units, thus having all the compression units compressing the same test result at the time same and providing that output to the parallel to serial converter for transfer, or if each

selected test result is provided to in some order to one of the compression units for compression and transfer though the parallel to serial converter.

As per claims 6, 7, and 12, it is unclear to the examiner how the results (and result signatures) are transferred to the scan chains (and blocks) when the results were produced from the scan chains (and blocks). Examiner notes this issue was raised within the prior examination with respect to claims 1 and 6.

As per claim 12, it is unclear to the examiner how the "test pattern generation unit is initialized as the test pattern into scanning test patterns in..." three different modes. It is the examiner's understanding that what is intended is the test pattern generation unit is initialized in one of the three modes (failure pattern, failure shift register, or failure block) to generate corresponding test patterns to that of the test mode initialized.

Additionally, it is unclear to the examiner if in the failure shift register determination mode if a single compressed test result signature for each test pattern is transferred in order as in the failure pattern determination mode, or if there is a compressed test result signature transferred for each of the scan chains.

As per claim 14, the examiner does not understand the claim. The exclusive-OR unit in conjunction with the compression units and the serial converter is unclear. The compression unit dose not compress, however the parallel to serial converter receives compressed test result signatures from the compression units connected to the divided blocks in one of the scan chains, the exclusive-OR performs a logic operation on the block results and outputs a single value, and the compression units are connected to the exclusive-OR and the divided blocks in one of the scan chains yet are less in

number than the number of block test results. Examiner invites applicant to call examiner regarding this claim.

As per claim 15, the second limitation within the claim is unclear to the examiner. Specifically it is unclear if the entire block test result is inverted or a signal value within the block test result. Also, it is unclear how the block test pattern used to test the block is inverted and inserted into the resulting inverted block test result. Examiner invites applicant to call examiner regarding this claim.

Claims 2-18 are dependent upon claim 1 and therefore also inherits the 35 U.S.C. 112, second paragraph issues and may not be further considered on their merits.

Claims 8-11 and 15-18 are dependent upon claim 7 and therefore also inherit the 35 U.S.C. 112, second paragraph issues and may not be further considered on their merits.

Claim 13 is dependent upon claim 12 and therefore also inherits the 35 U.S.C. 112, second paragraph issues and may not be further considered on their merits.

Claims 16-18 are dependent upon claim 15 and therefore also inherits the 35 U.S.C. 112, second paragraph issues and may not be further considered on their merits.

Claims 4, 5, 9, 10, and 11 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the compressing of the test results between the "receiving the (block) test results," and "and to transfer the

compressed (block) test result signatures," since the compressing must take place within the compression units of these claims prior to the transferring of compressed test results.

Examiner strongly advises applicant to review the claims for any further issues within the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1,2, 6, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Coteet at (US Patent 6671839 B1).

1. As per claim 1, Coteet teaches an integrated circuit comprising:

Scan chains implemented by registers disposed in a logic circuit, configured to shift in test patterns, to transfer the test patterns to the logic circuit, to receive test results of the logic circuit, and to shift out the test results (column 1 lines 14-18, column 3 lines 46-60 with figure 2, and column 4 lines 4-12 with figure 2);

A test pattern generation unit configured to transform the test patterns as scanning test patterns for feeding into the scan chains (column 1 lines 20-26, column 3 lines 46-60, and column 7 lines 10-19); and

A test result compression unit connected to the output stages of the scan chains, configured to compress the test results so as to generate the same number of compressed test result signatures as the number of the test results, to transfer the resulting compressed test result signatures with the scan chains in a first order at allow one-to-one mapping, and to detect the scan chain which fails to match the compressed test result signature corresponding to each scan chain (column 1 lines 20-26, column 3 lines 46-60 and column 4 lines 12-16).

2. As per claim 2, Coteet teaches the integrated circuit further comprising:

An expected value comparison circuit configured to compare the compressed test result signatures with a corresponding expected value in order, and detects a compressed test result signature which fails to match the corresponding expected value (column 4 lines 10-16, column 1 lines 20-25, and column 3 lines 50-54).

3. As per claim 6, Coteet teaches the integrated circuit wherein the test result compression unit comprises:

A mode changeover circuit connected to the output stages of the scan chains configured to receive the test results in parallel and output the test results in parallel in a self-test mode, to receive the test results in parallel in a failure analysis mode, and to transfer the test results to the scan chains in a first order

that allows one-to-one mapping (figure 2, column 1 lines 13-26, column 3 lines 45-55, and column 4 lines 10-16); and

A data compression unit connected to the mode changeover circuit configured to receive the test results in parallel in the self-test mode, to collectively compresses the test results into a single compressed test result signature, and to compresses the test results in the first order in the failure analysis mode (column 1 lines 20-26, column 3 lines 45-55, and column 4 lines 10-16).

4. As per claim 7, Coteet teaches the integrated circuit wherein the test pattern generation unit divides the test pattern, generating scanning test patterns;

The scan chains shift in the scanning test patterns and simultaneously transfer the scanning test patterns to the logic circuit, receive the test results from the logic circuit, and shift out block test results dividing the test results from respective last stages of block in the scan chains (column 7 lines 10-19); and

The integrated circuit further comprising a block compression unit configured to receive the block test results, to compress the test results so as to generate the same number of compressed test result signatures as the test results, and to transfer the resulting compressed block test result signatures to the blocks in order that allows one-to-one mapping (column 1 lines 20-25, column 3 lines 45-55, column 4 lines 10-15).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 3, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteet at. (US Patent 6671938 B1) as applied to claims 1-2 above, and further in view of Sager et al (US Patent 4342084).

5. As per claims 3, 12, and 13, Coteet teaches the integrated circuit as described above in detail, comprising: scan chains, a test pattern generator (TPG), a test result compression unit, and an expected value comparison unit. Taught by Coteet yet not described above in detail are counters within the integrated circuit, pattern and bit counters (figure 2 and columns 3-4 lines 65-2). Also taught in Coteet are changes in test mode and parallel processing (see figure 2).

Coteet does not specifically teacher wherein the integrated circuit further comprising:

A failure scan chain determination circuit configured to count the order of a compressed test result signature which fails to match the corresponding

expected value during comparison in order, and determines a failure scan chain, which includes a failure detected in the scan chains.

However in an analogous art Sager teaches the need to replace or repair parts/components that have not past testing or that have resulted a circuit/device under test (DUT) to not pass testing, wherein the determination of passing or not passing testing is dependent upon the value or magnitude of errors detected and counted. The art is replete with such references that teach this, Sager is but one.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to modify Coteet's teachings so that a counter count errors detected such as taught by Sager so that the expected value comparison unit can expedite test execution and thus expedite the execution of repair or replacement of faulty scan chains since additional time does not need to be spent on analyzing further data from a scan chain when the magnitude of errors exceeds the value in which it does not pass the testing.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteet at. (US Patent 6671938 B1) as applied to claim 1 above.

6. As per claim 4, Coteet teaches the integrated circuit wherein the test result compression unit includes:

Data compression units connected to the respective output terminals of the scan chains, configured to receive the test results, and to transfer the compressed test result signatures, the number of the data compression units is

the same as the number of the test results (column 3 lines 45-55 and column 4 lines 25-30)

Coteet does not specifically teach wherein the test result compression unit includes:

A parallel to serial converter connected to all of the data compression units, configured to receive the compressed test result signatures in parallel, and to serially transfer the compressed test result signatures in order.

However Coteet does disclose a space compactor used to reduce the number of inputs to the MISR (column 4 lines 25-30). It would have been obvious to one having ordinary skill in the art at the time the invention was made to increase this reducing of a number of inputs down to a single input since the examiner take official notice of the equivalence of the space compactor and a parallel to serial converter for their use in the reduction of connections required art and the selection of any of these know equivalents to reduce pins and complexity of system connections would be within the level of ordinary skill in the art.

Furthermore, Coteet teaches the space compactor used prior it input to data compression. It would have been obvious to one having ordinary skill in the art at the time the invention was made to reposition the space compactor is being used after data compression, since is has been held that mere reversal of the essential working parts of a device involves only routine skill in the art.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to reverse the order of the compression unit and the

recognized equivalent space compactor within Coteet, wherein the space compactor placed prior to the compression unit is limiting efficiency by restricting the flow of data to the compression unit which provides less data output. The less data output by the compression unit would thus reduce or eliminate any restriction of data flow by the space compactor if placed after data had been compressed.

7. As per claim 5, Coteet teaches the integrated circuit wherein the test result compression unit comprises:

A selector connected to the output terminals of the scan chains, configured to select and transfer the test results in order (column 4 lines 25-30).

Coteet does not specifically teach wherein the result compression unit comprises:

A plurality of data compression units connected to the first selector configured to receive the test results, and to transfer the compressed test result signatures, the number of the data compression units being smaller than the number of the test results; and

A parallel to serial converter connected to the data compression unit configured to receive the compressed test result signatures in parallel, and to serially transfer the compressed test result signatures in order.

However Coteet teaches a data compression unit (column 3 lines 45-55 and column 1 lines 23-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate the data compression unit to perform parallel processing and thus reducing execution time, since it has been held that mere

duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co., 193* USPQ 8.

Furthermore, the parallel to serial converter and its location after the data compression unit configured to receive the compressed test result signature in parallel, and to serially transfer the compressed test result signature in the first order has been covered in the preceding claim, as per claim 4 as described in detail above.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to duplicate the data compression unit and reverse the order of the multiple compression units and the recognized equivalent space compactor within Coteet, wherein the space compactor placed prior to the compression unit is limiting efficiency by restricting the flow of data to the compression unit which provides less data output. The less data output by the compression unit would thus reduce or eliminate any restriction of data flow by the space compactor if placed after data had been compressed.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coteet at. (US Patent 6671938 B1) as applied to claims 1 and 7 above, and further in view of Sager et al (US Patent 4342084).

8. As per claim 8, Coteet teaches the integrated circuit further comprising:

A block expected value comparison circuit configured to compare the compressed block test result signature with the corresponding expected value in order, and to detect a compressed block test result signature that fails to match

the corresponding expected value (column 3 lines 45-55, column 1 lines 25-35, and column 4 lines 10-16).

Coteet does not specifically teach wherein the integrated circuit further comprises:

A failure block determination circuit configured to count the order of the compressed block test result signature that fails to match the corresponding expected value in order, and to identify a failure block having a failure detected in the blocks.

However in an analogous art Sager teaches the need to replace or repair parts/components that have not past testing or that have resulted a circuit/device under test (DUT) to not pass testing, wherein the determination of passing or not passing testing is dependent upon the value or magnitude of errors detected and counted. The art is replete with such references that teach this, Sager is but one.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to modify Coteet's teachings so that a counter count errors detected such as taught by Sager so that the expected value comparison unit can expedite test execution and thus expedite the execution of repair or replacement of faulty scan chains since additional time does not need to be spent on analyzing further data from a scan chain when the magnitude of errors exceeds the value in which it does not pass the testing.

Claims 9, 10, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteet at. (US Patent 6671938 B1) as applied to claims 1 and 7 above.

9. As per claims 9, 10, and 11, Coteet teaches the integrate circuit as described above in detail as per claims 1 and 7.

Coteet does not specifically teacher wherein the block compression unit comprises:

> Data compression units, connected to the output terminals of the blocks, configured to receive the block test results, and to transfer compressed block test result signatures, the number of the data compression units is the same as the number of the block test results, and
>
> A parallel to serial converter configured to receive in parallel the compressed block test result signature from the data compression units, which are connected to the divided blocks in one of the scan chains, and to serially transfer the compressed block test result signatures in order.

However Coteet does teach of a compression unit and an art recognized equivalent to a parallel to serial converter, as described above as per claim 4. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate these components within the integrated circuit, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.,* 193 USPQ 8.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to duplicate these essential components within the intergraded circuit as taught by Coteet since it would implement parallel processing of data which as is well know would decrease the processing time required by the integrated circuit to execute or process data.

10. As per claim 14, Coteet teaches the integrate circuit wherein the block compression unit comprises:

An exclusive-OR calculation unit configured to transfer an exclusive-ORed value of the block test results, which are delivered from the scan chains including a failure scan chain (column 4 lines 18-21). Examiner notes that a LFSR is well known to have logic gates within used to either help expand or compress data.

Coteet does not specifically teacher wherein the integrated circuit wherein the block compression unit comprises:

Data compression units connected to the exclusive-OR calculation unit, configured to receive the exclusive-ORed value, and to transfer the compressed block result signatures, the number of the data compression units is smaller that then number of the block test results; and

A parallel to serial converter configured to receive in parallel the compressed block test result signatures from the data compression unit connected to the divided blocks in one of the scan chains and to serially transfer the compressed block test result signatures in order.

However Coteet does teach of a compression unit and an art recognized equivalent to a parallel to serial converter, as described above as per claim 4. It would have been obvious to one having ordinary skill in the art at the time the invention was made to duplicate these components within the integrated circuit, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.,* 193 USPQ 8.

Therefore one of ordinary skill in the art at the time the invention was made would have been motivated to duplicate these essential components within the intergraded circuit as taught by Coteet since it would implement parallel processing of data which as is well know would decrease the processing time required by the integrated circuit to execute or process data.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2117

CYNTHIA BRITT
PRIMARY EXAMINER
6-7-07